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Porto Alegre, Brazil Abstract : This paper deals with reusability issues in the development of a double data rate (DDR) SDRAM controller ... or VHDL adds some benefits to the design as it: Uses ...

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DDR SDRAM Controller IP Designed for Reuse

The most interesting part of this board is of course the inclusion of the FPGA which left us wondering what the code for the device ... DEV_UART 1 08000000 MB_DEV_SDRAM 4 09000000 MB_DEV_NP ...

Hands-On With New Arduino FPGA Board: MKR Vidor 4000

By itself that isn't that interesting, but the Sno also has an Altera/Intel Max 10 FPGA ... like SDRAM. If you are looking for a project, it might be interesting to convert our PWM code into ...

Tiny Arduino + FPGA = Sno

The SDRAM Controller is also available in source code (VHDL or Verilog) with a testbench. Customers can evaluate the SDRAM Controller for free prior to licensing as an Altera's OpenCore(tm) Netlist or ...

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